IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Robert L. Hodges, et al.	Art Unit:	Unassigned
Serial Number:	Unassigned	Examiner:	Unassigned
Filed:	HereWith		
Title:	Semiconductor Device With Deposited Oxide		
Date:	Jan. 18, 2002		

Assistant Commissioner For Patents
Washington DC 20231

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified patent application as follows:

In the Specification:

Please delete paragraph 5.

Please replace paragraph 38 with the following paragraph. A marked-up version of paragraph 38 is enclosed herein.

--Cavitation barrier layer 142, barrier layer 158, and nozzle plate 160 define a firing chamber 148 having nozzle 150 providing an opening thereto. Electrical contact 144 is upon cavitation barrier layer 142. The ink jet print head seen in Figure 13 is in communication with a thermal ink jet printer 156 through a lead 154 to electrical contact 144. Figure 13 can be compared to Figure 6b in that gate electrodes 42 of Figure 6b are electrically isolated one from another by deposited oxide layer 44 there between which also prevents current from flowing between active region 38 of the first FET and active region 37 of the second FET. Similarly, gate electrode 120 of Figure 13 is electrically isolated from other gate electrodes by deposited oxide layers 118a, 118b on opposite sides of gate electrode 120. Such other gate electrodes

having associated active regions can be situated upon semiconductor substrate 102 adjacent to the gate electrode 120 in Figure 13. As such, deposited oxide layers 118a, 118b prevent current from flowing between each of the primary and secondary active regions 108, 114 to any active region that is respectively adjacent thereto.--

Respectfully Submitted,

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Encl: Marked up paragraph 38

Marked up Paragraph 38:

--Cavitation barrier layer 142, barrier layer 158, and nozzle plate 160 define a firing chamber 148 having nozzle 150 providing an opening thereto. Electrical contact 144 is upon cavitation barrier layer 142. The ink jet print head seen in Figure 13 is in communication with a thermal ink jet printer 156 through a lead 154 to electrical contact 144. Figure 13 can be compared to Figure 6b in that gate electrodes 42 of Figure 6b are electrically isolated one from another by deposited oxide layer 44 there between which also prevents current from flowing between active region 38 of the first FET and active region 37 of the second FET. Similarly, gate electrode 120 of Figure 13 is electrically isolated from other gate electrodes by deposited oxide layers 118a, 118b on opposite sides of gate electrode 120. Such other gate electrodes having associated active regions can be situated upon semiconductor substrate 102 [to the left and to the right of] adjacent to the gate electrode 120 [with respect to] in Figure 13. As such, deposited oxide layers 118a, 118b prevent current from flowing between each of the primary and secondary active regions 108, 114 to any active region that is respectively adjacent thereto.--